**Introduction to Digital Design (55:032)**
**(Required: All Tracks)**

**Catalog Description:**
Modern design and analysis of digital switching circuits; combinational logic; sequential circuits and system controllers; interfacing and busing techniques; design methodologies using medium- and large-scale integrated circuits; lab arranged. Prerequisite: sophomore standing.

**Pre(co)requisites:**
Sophomore standing

**Textbook:**
Mano & Kime, *Logic and Computer Design Fundamentals, Forth Edition*, Prentice Hall, 2008

**References:**
Xilinx references on course website

**Topics (Class Hours):**
1. Introduction to digital systems (1)
2. Information representation (3)
3. Logic operations and combinational circuits (5)
4. Combinational logic synthesis (5)
5. Hardware Description Language (6)
6. Sequential circuits (7)
7. Registers, memory, programmable logic devices (6)
8. Register Transfer Level (RTL)specification and design (4)
9. Sequencing and control (4)
10. Basic computer architecture (2)
11. In class exams (2)

**Laboratory Projects:**
1. Introduction to lab equipment--build and test a simple digital circuit using TTL ICs.
2. Combinational circuit design using switches, TTL gates, LEDs
3. Combinational circuit design using VHDL and programmable gate array (FPGA)
4. 4-bit ALU design using VHDL and FPGA
5. Integrating counter design using sequential VHDL and FPGA
6. 4-wheel robot control unit using sequential VHDL and FPGA

**Class/Laboratory Schedule**:
Three 50-minute lectures per week; six three-hour lab sessions during the semester

**Writing Assignments and Oral Presentations:**
Written reports, in a specified standard format, are required for labs.

**Design Component:**
Beginning with laboratory project #2 listed above, the students are given the requirements for a digital logic circuit that they must design and verify. The complexity of the design assignments

range from a simple combinational logic circuit through a moderately complex 4-wheel robot control unit that must autonomously navigate a maze. All assignments except for laboratory project #2 are implemented using VHDL and an FPGA development unit.

**Contribution to the Requirements of Criterion 5:**
Engineering topics: 3 s.h.

**Course Goals: Basis for Assessment and Mapping onto Outcomes**

| Course Goal | Basis For Goal Assessment | Supports ABET Outcomes |
|---|---|---|
| 1. Understanding of digital information representation and arithmetic. | Homework, exam questions | a(●), e(●), k(●) |
| 2. Understanding of the structure and design of combinational logic circuits | Homework, exam questions, lab reports | a(●), c(●), e(●), k(●) |
| 3. Understanding of sequential logic circuits | Homework, exam questions, lab reports | a(●), c(●), e(●), k(●) |
| 4. Understanding of Hardware Description Language and associated tools | Lab reports | a(●), c(●), e(●), j(●) k(●) |
| 5. Understanding of modern programmable logic devices | Homework, exam questions, lab reports | a(●), c(●), e(●), j(●), k(●) |
| 6. Understanding of Register Transfer Level Operations | Homework, exam questions, lab reports | a (●), c(●), e(●), k(●) |
| 7. Understanding of basic computer system architecture. | Homework, exam questions, lab reports | a(●), e(●), k(●) |
| 8. Have opportunities to further his/her professional development through working on teams in laboratory projects; practicing written, oral and graphical communication skills; and using modern computer tools. | Lab reports | b(○), d(○), g(○), k(○) |

◦ denote moderate contribution to the outcome; • denote substantial contribution to the outcome

**Performance Criteria:**
Instructor completes a Course Outcome Rating (COR) that quantitatively evaluates student performance for each course goal-related outcome using a standard scale (4.0 = outstanding ability; 3.0 = good ability; 2.0 = adequate ability; 1.0 = poor ability; 0.0 = no ability). Instructor chooses appropriate graded course artifacts (homework questions, exam questions, etc) for each outcome rating. COR scores below 2.5 are indicative of problems with meeting course goals/outcomes and COR scores below 2.0 indicate failure to adequately meet course goals/outcomes.

**Prepared By:**
James Maxted (July, 2008)