

Computer Architecture and Organization (55:035)
(Required: Computer Engineering Track)

Catalog Description:

Basic concepts: computer evolution, register transfer-level design, simulation techniques, instruction sets (CISC and RISC), assembly language programming, ALU design, arithmetic algorithms and realization of arithmetic functions, hardwired and microprogrammed control; memory hierarchies: virtual memory, cache memory; interrupts and DMA; Input/output; introduction to high-performance techniques: pipelining, multiprocessing; introduction to hardware description languages (Verilog, VHDL): students design and simulate a simple processor. Offered spring semesters.

Pre(co)requisites:

057:017 [P], 055:032 [P]

Textbook:

Hamacher, Vranesic, and Zaky: Computer Organization, Fifth Edition, McGraw Hill, 2002. (ISBN 0-07-232086-9)

References:

Various materials on class web site

Topics (Class Hours):

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|---|---|
| 1. Computer system history and overview (3) | 6. Control unit and datapath design (7) |
| 2. Instruction set architecture and assembler programming (6) | 7. Memory system basics (2) |
| 3. Instruction set case studies (5) | 8. Cache memory (3) |
| 4. Computer Arithmetic and ALU design (8) | 9. Virtual Memory (2) |
| 5. Hardware description language (Verilog) (4) | 10. Input/Output system design (2) |
| | 11. Exams (2) |

Laboratory Projects:

None

Class/Laboratory Schedule:

Three 50-minute lectures per week

Writing Assignments and Oral Presentations:

None

Design Component:

Homework assignments require students to complete open-ended design exercises. In addition, students are required to complete two system design projects using the Verilog hardware description language. These projects involve designing, implementing, and testing a simple processor.

Contribution to the Requirements of Criterion 5:

Engineering topics: 3 s.h.

Course Goals: Basis for Assessment and Mapping onto Outcomes

Course Goal	Basis For Goal Assessment	Supports ABET Outcomes
1. The student will understand the fundamentals of computer instruction set architecture, including machine-level instruction formats and addressing modes.	Homework, Exam questions, projects	j(●), k(●)
2. The student will understand the difference between RISC and CISC instruction sets	Homework, exam questions	c(●), e(●), j(●), k(●)
3. The student will understand binary number representations and binary arithmetic.	Homework, exam questions	a(●), j(●), k(●)
4. The student will be able to write, encode, and run a simple assembler program on a conceptual processor.	Homework	c(●), j(●), k(●)
5. The student will understand basic algorithms and hardware structures for performing integer computer arithmetic (addition, subtraction, multiplication, and division).	Homework, exam questions	c(●), j(●), k(●)
6. The student will understand floating point format for representation of real numbers in a computer	Homework, exam questions	c(●), j(●), k(●)
7. The student will understand basic algorithms and hardware structures for addition and multiplication of floating point numbers.	Homework, exam questions	c(●), j(●), k(●)
8. The student will have basic facility with a modern hardware description language and will be able to use it to specify, simulate, and analyze aspects of a computer system design.	Projects	a(●), c(●), e(●), j(●), k(●)
9. The student will understand the basic structure and organization of a processor datapath.	Homework, exam questions, projects	c(●), j(●), k(●)
10. The student will understand the function of the control unit in a processor and will be able to design a control unit for a simple processor.	Projects	c(●), e(●), j(●), k(●)
11. The student will understand the basic operation of the memory system of a computer.	Homework, exam questions	e(●), j(●), k(●)
12. The student will understand the principles of cache memory systems, including direct mapped, set-associative, and fully associative cache organizations.	Homework exam questions	c(●), e(○), j(●), k(●)
13. The student will understand the basic notions of paged and segmented virtual memory systems and their relationship to processor architecture.	Homework, exam questions	c(●), e(○), j(●), k(●)
14. The student will understand the basic principles of the input/output subsystem of a computer including interrupt-driven I/O and DMA.	Homework, exam questions	c(●), e(○), j(●), k(●)

○ denote moderate contribution to the outcome; ● denote substantial contribution to the outcome

Performance Criteria:

Instructor completes a Course Outcome Rating (COR) that quantitatively evaluates student performance for each course goal-related outcome using a standard scale (4.0 = outstanding ability; 3.0 = good ability; 2.0 = adequate ability; 1.0 = poor ability; 0.0 = no ability). Instructor chooses appropriate graded course artifacts (homework questions, exam questions, etc) for each outcome rating. COR scores below 2.5 are indicative of problems with meeting course goals/outcomes and COR scores below 2.0 indicate failure to adequately meet course goals/outcomes.

Prepared By:

Jon Kuhl (October, 2007)