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Introduction to VLSI Design

Implementation Options

Adapted from Weste and Harris notes

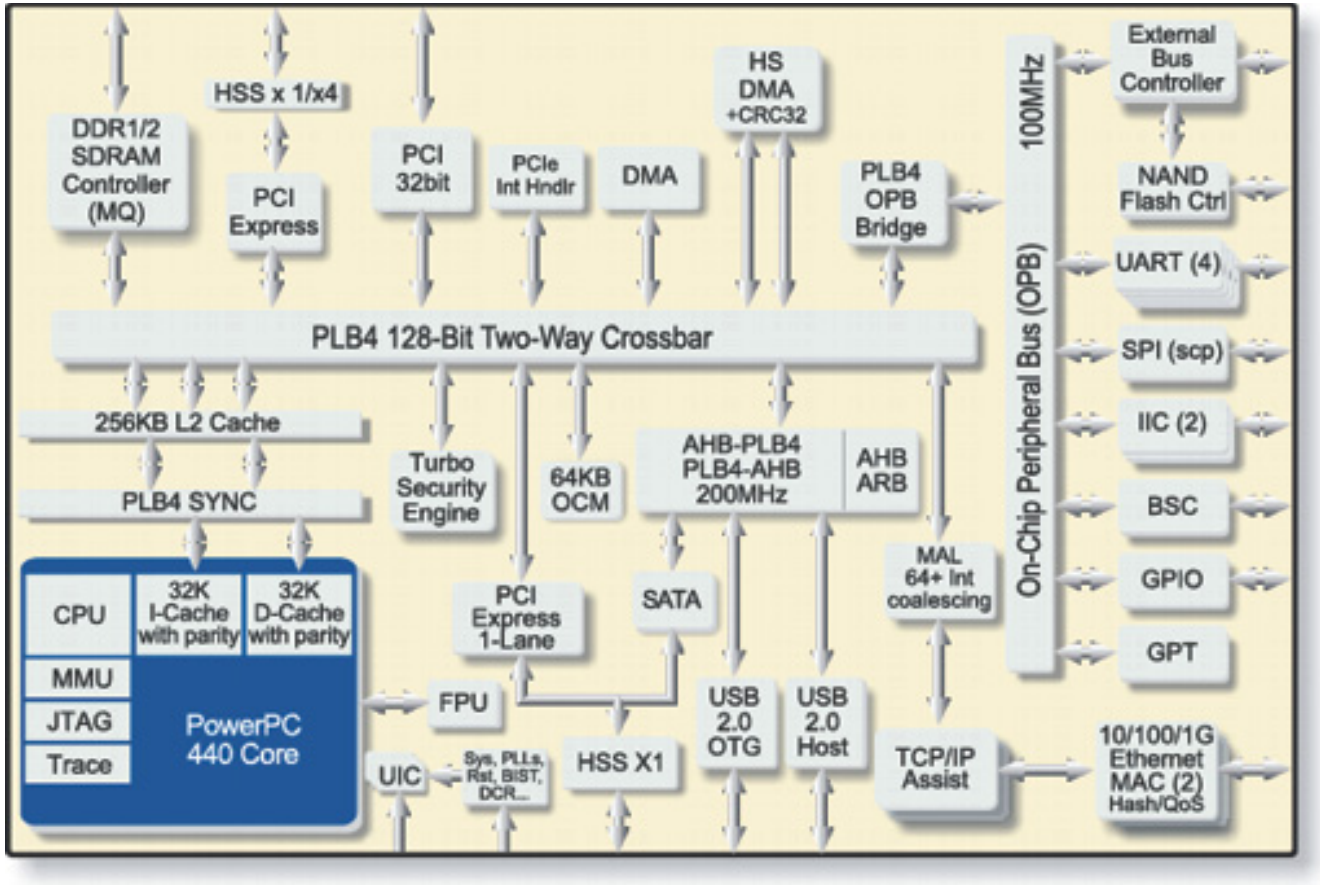
Implementation Options

- Use an existing chip
- Field Programmable Gate Array
- Sea of Gates/Gate Array
- Standard Cell
- Full Custom

Implementation Options

- Use an existing chip
  - Pros
    - Minimal hardware development cost – hardware is “done”!
  - Cons
    - May need a (big) software development!
    - Other features may not be a great fit
    - Beware of performance limitations
    - Beware of power consumption
    - Don’t forget about other hardware (memories, PHYs, etc)
  - Examples
    - Off-the-shelf microprocessor
    - Application Specific device

Applied Micro PPC460EX

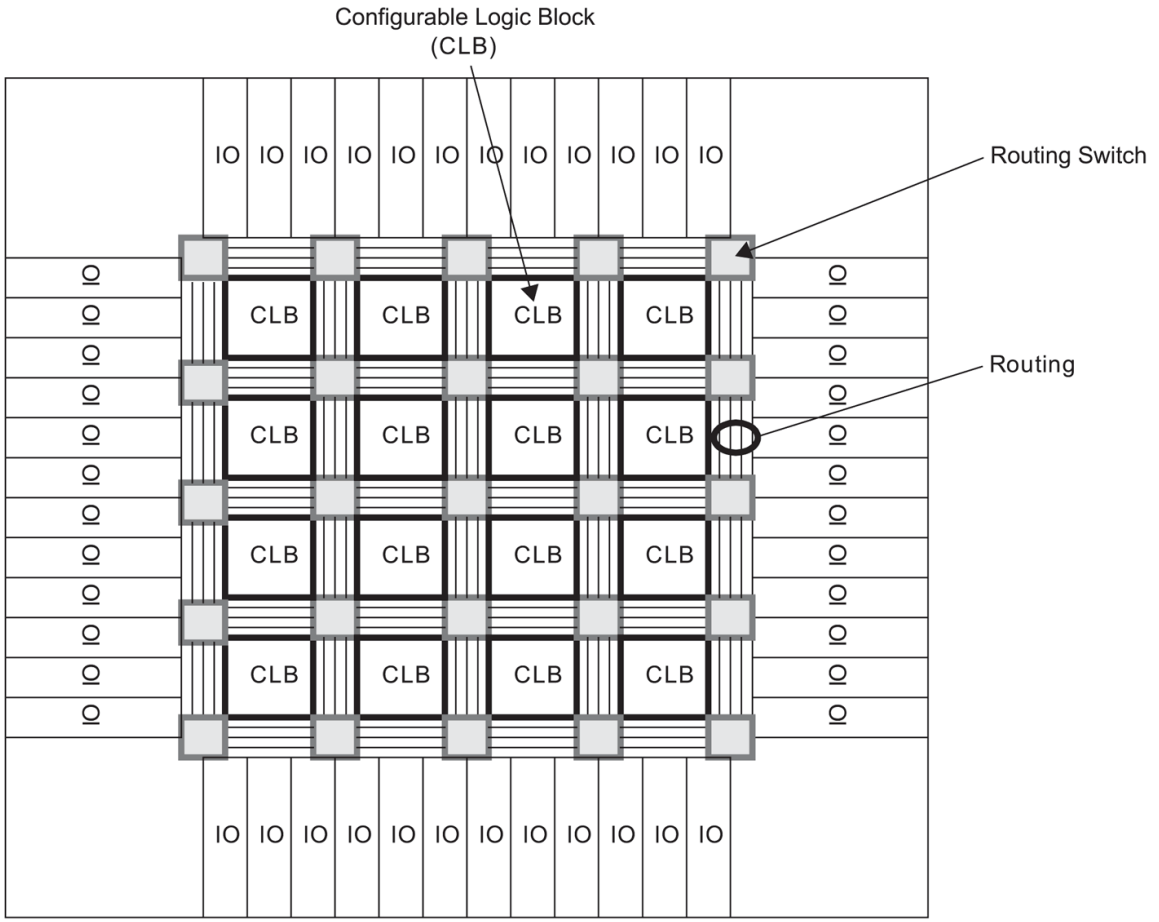


Courtesy of Applied Micro (APM)

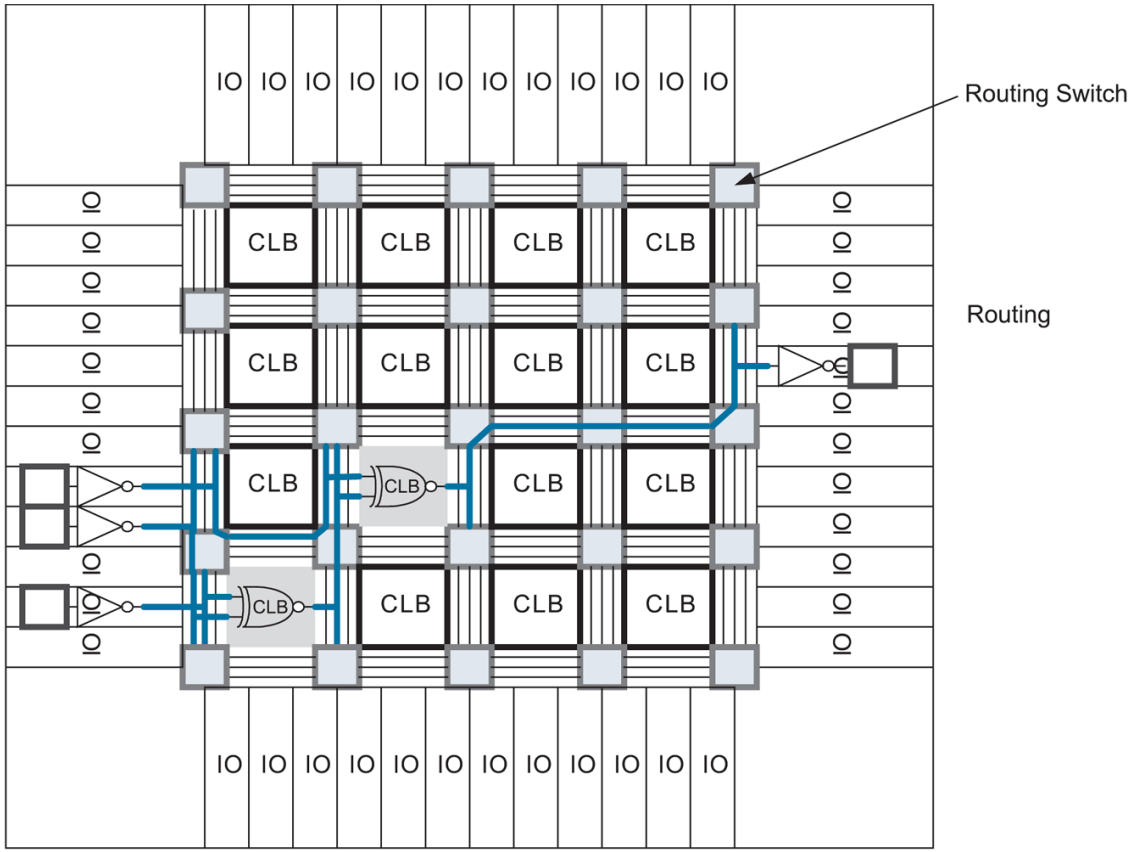
Implementation Options

- FPGAs or PLDs
  - Pros
    - Back-end (fabrication) is done
      - Saves time and money
  - Cons
    - Clock rate usually won't match that of a Gate Array/Std Cell
    - Usually has higher recurring cost
    - "Fixed" feature set (RAM, PLLs, etc) may limit your options
  - Examples
    - RAM-based FPGA from Xilinx or Altera
    - Flash-based FPGA from Actel

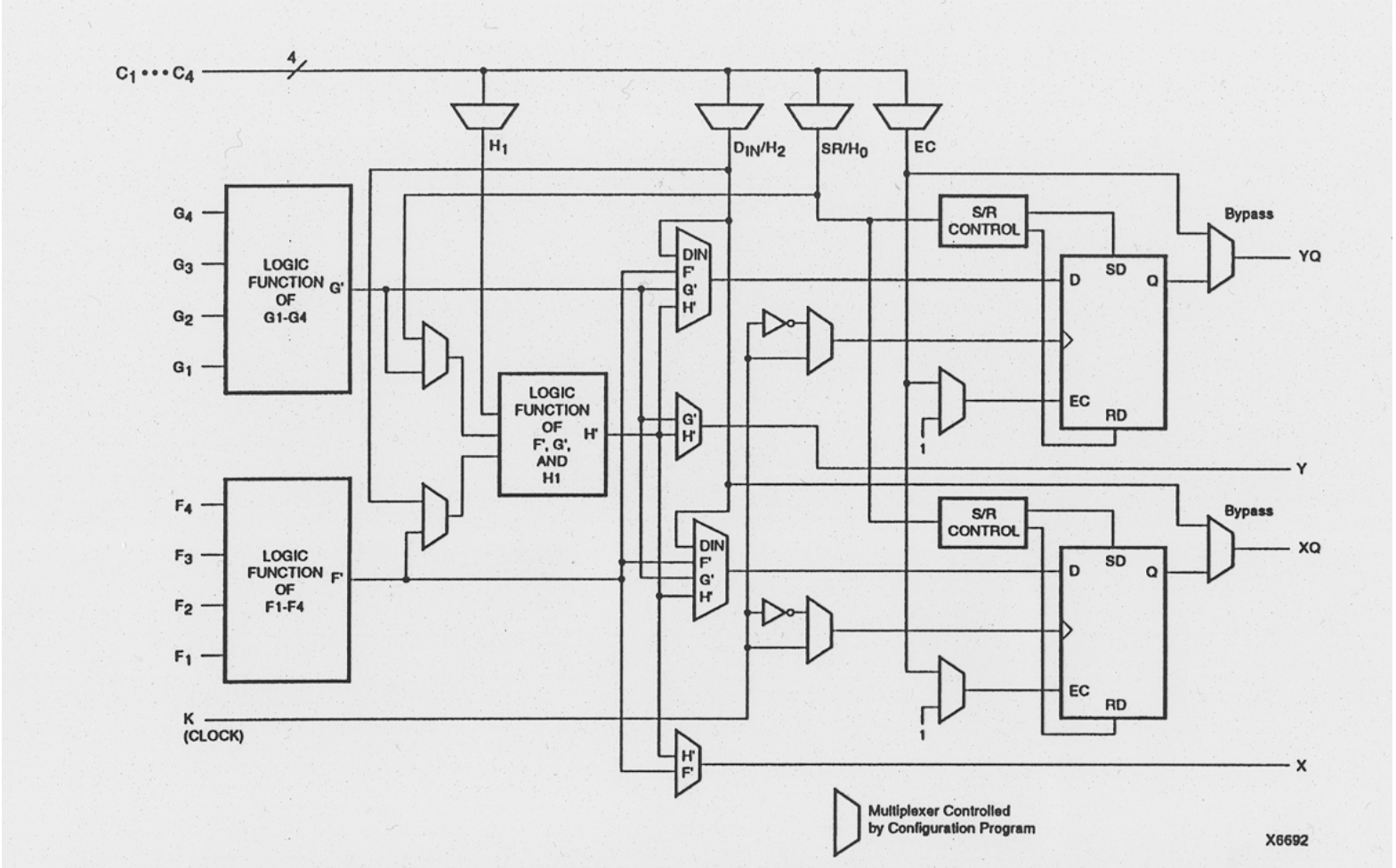
Simplified FPGA Floorplan



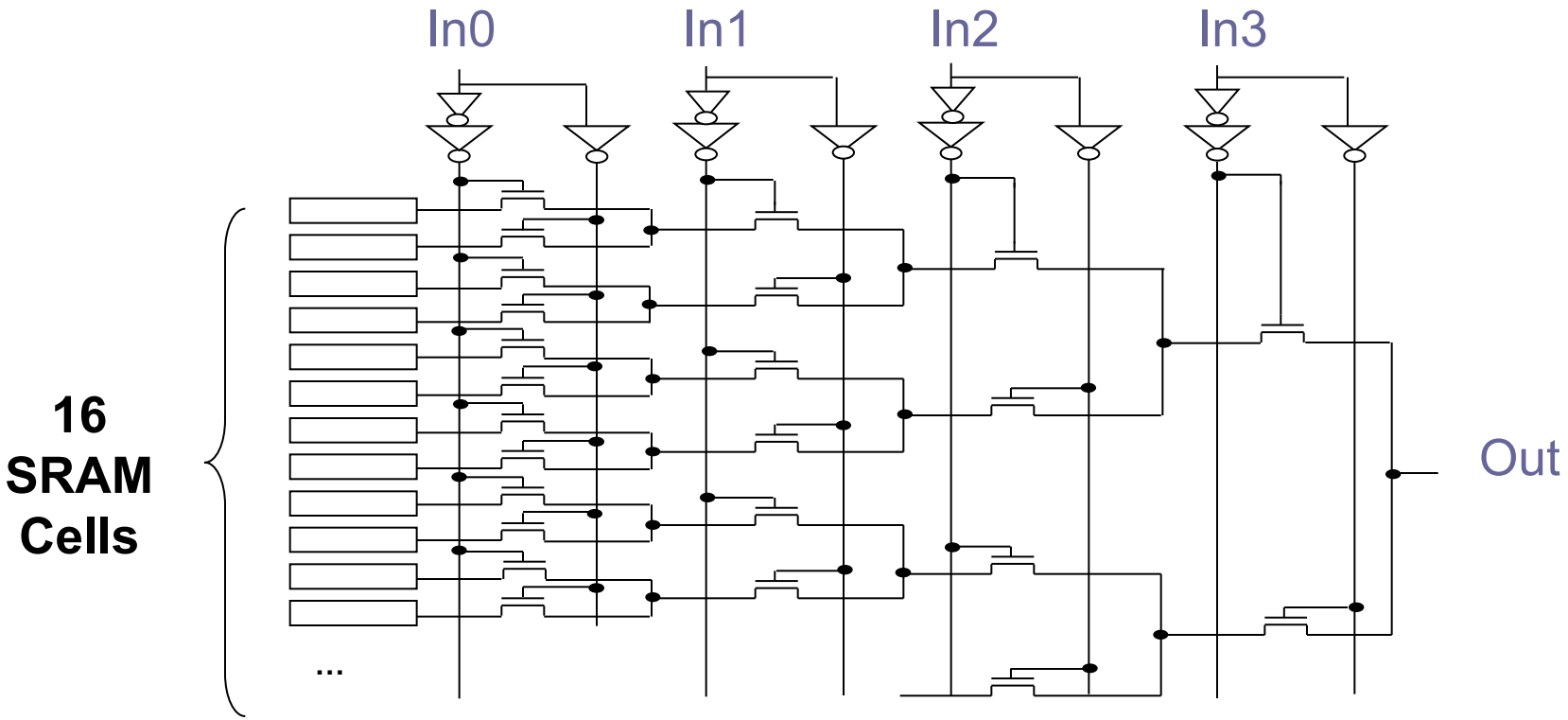
“Configured” FPGA



Xilinx CLB – a.k.a. "Slice"



4-input Look-up Table Implementation

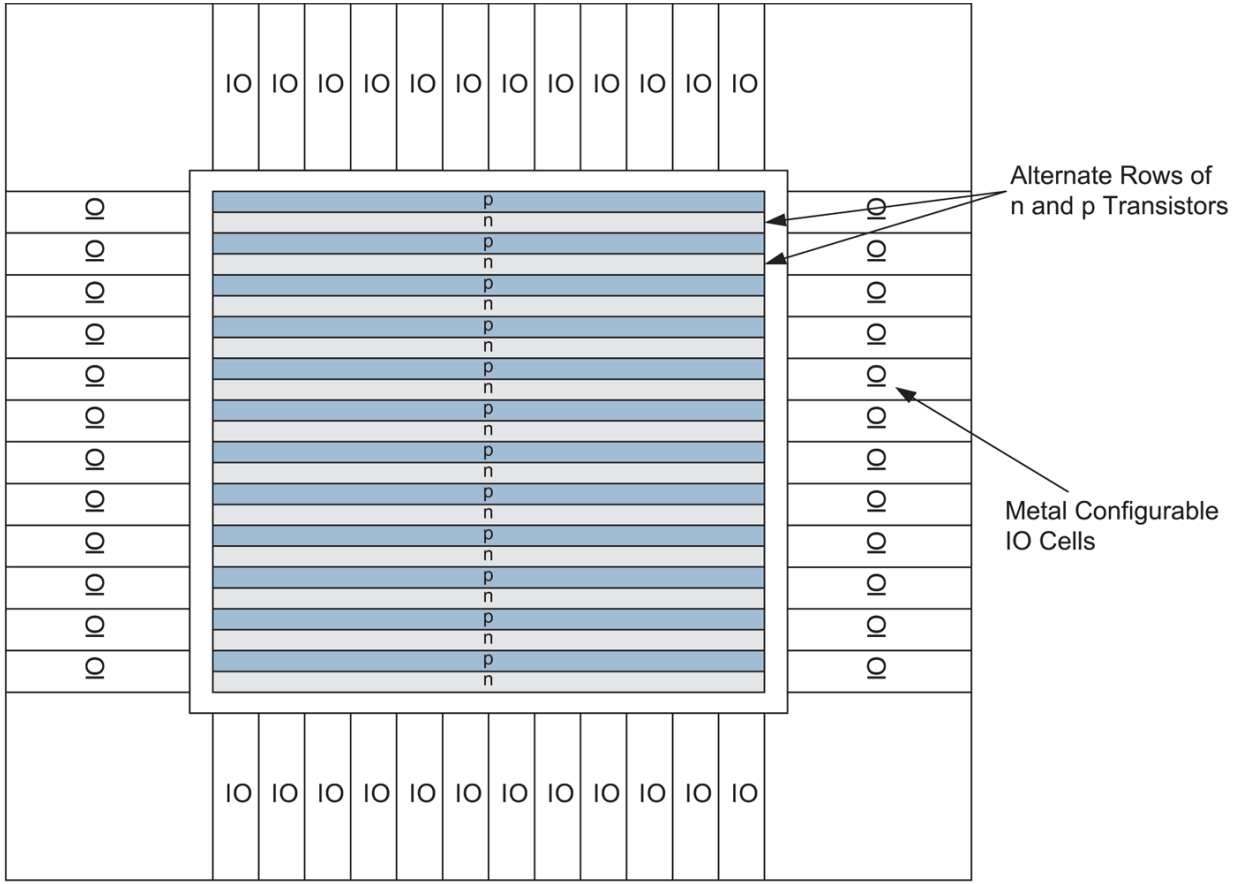


Out = f (in0, in1, in2, in3)

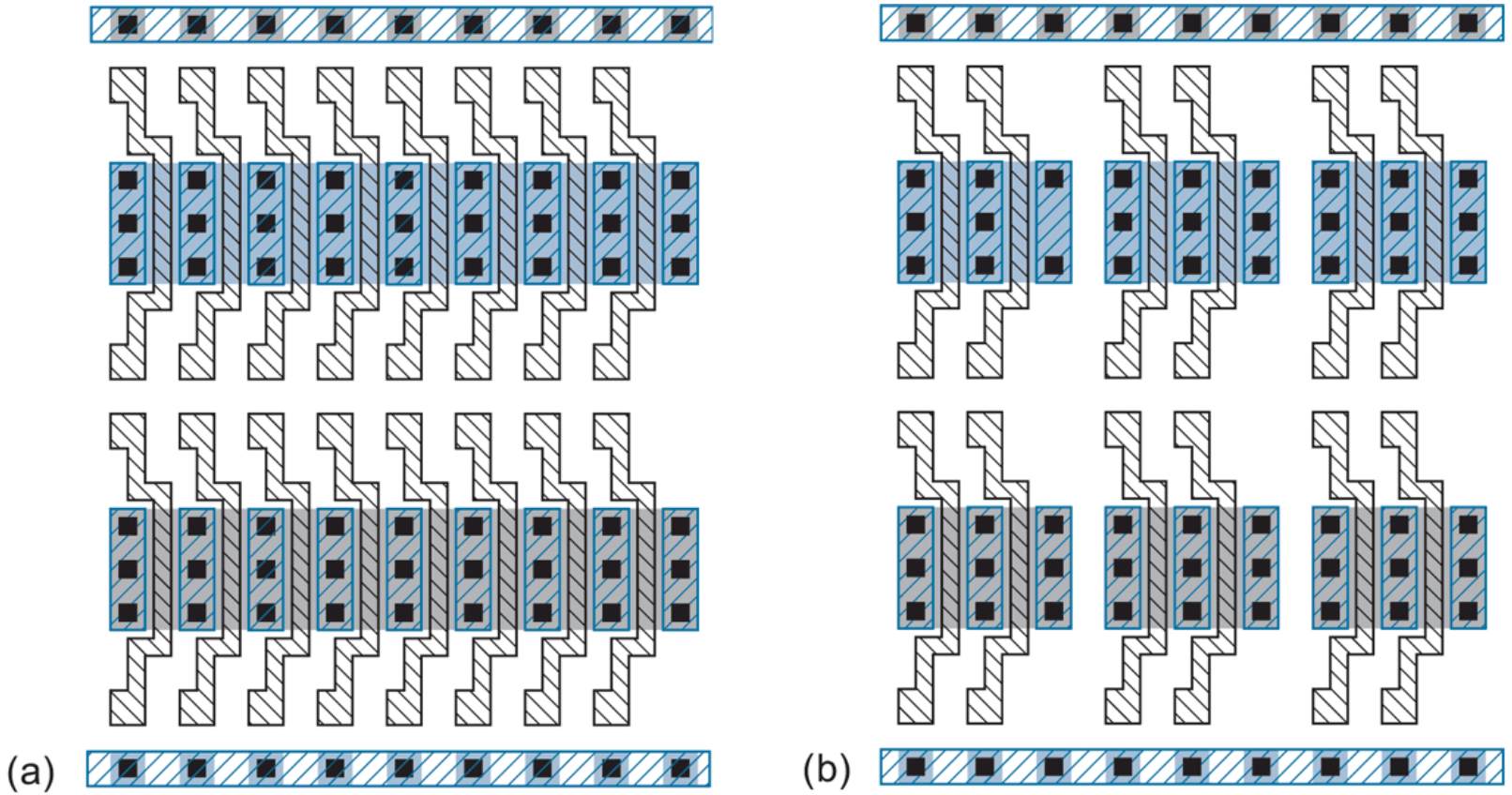
Implementation Options

- Sea of Gates/Gate Array
  - Pros
    - Much of the fabrication is done
      - Base wafers have transistors and memories done
      - “User”-defined logic implemented in (a few) metal layers
    - Lower development costs than Standard Cell because supplier can amortize mask costs over all base array designs
    - Better clock rate and lower power than FPGA
  - Cons
    - Clock rate usually won’t match that of a Std Cell
    - “Fixed” feature set (RAM, PLLs, etc) may limit your options
  - Examples
    - LSI Logic LCA500K

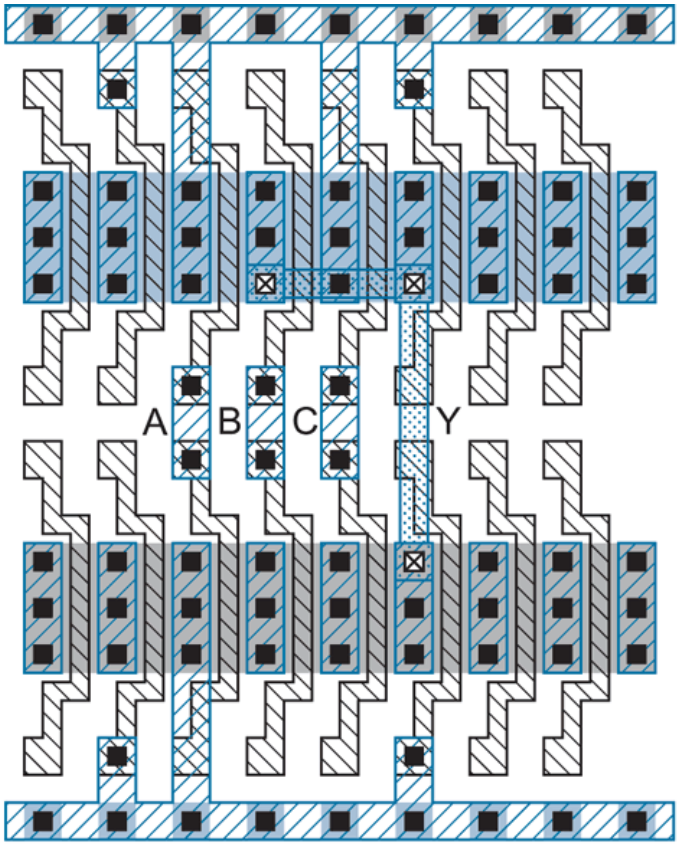
Simplified Sea of Gates Floorplan

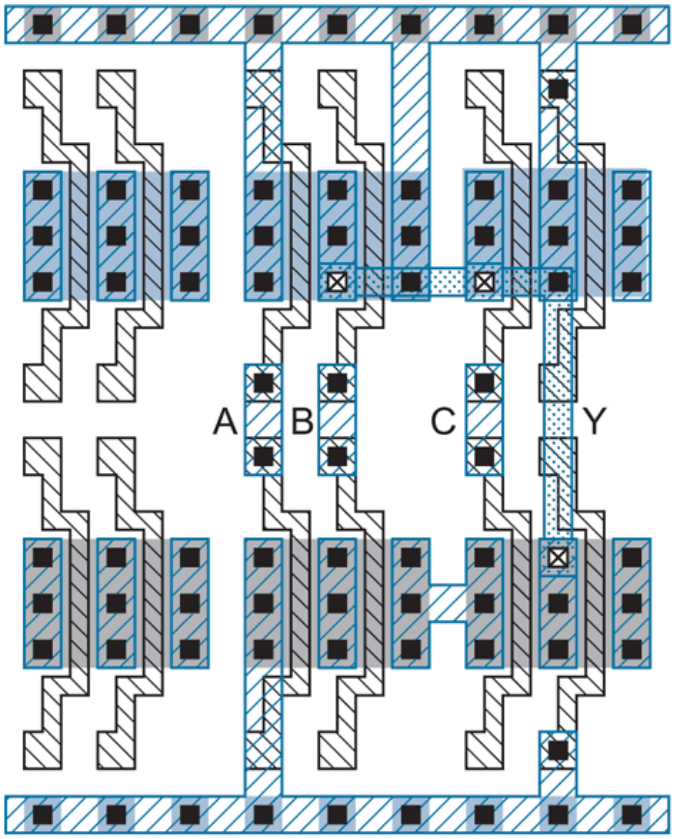


SoG and Gate Array Cell Layouts



SoG and Gate Array 3-in NAND

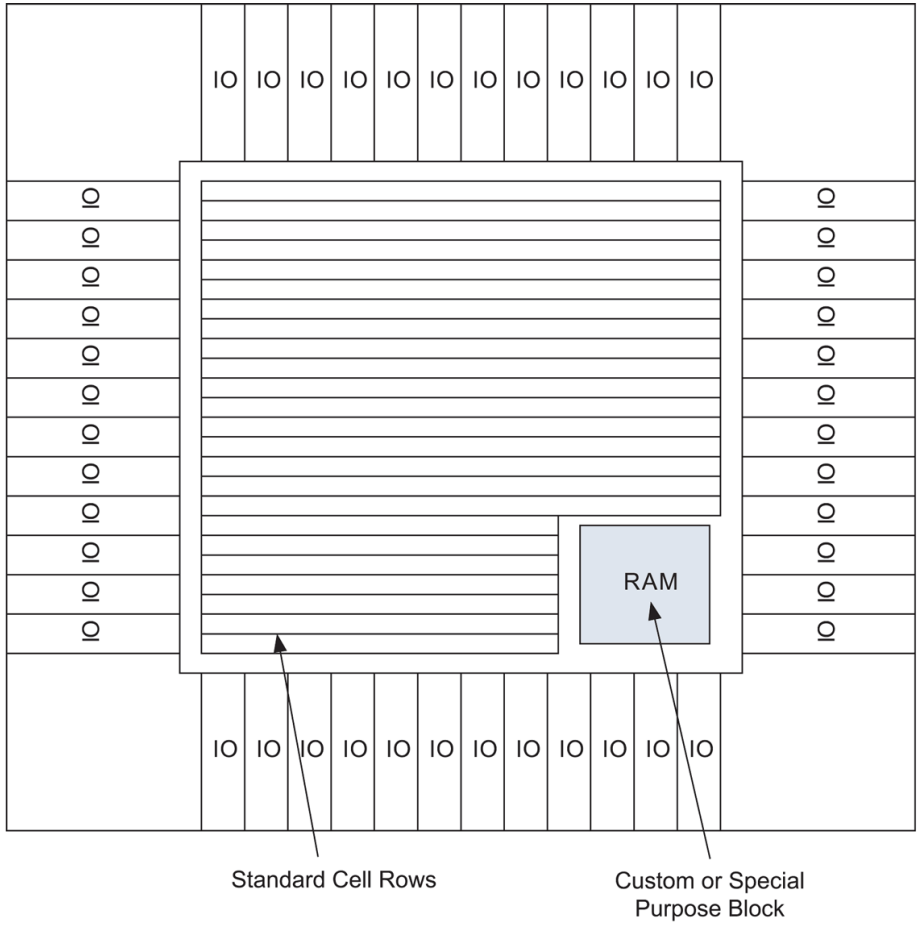




Implementation Options

- Standard Cell
  - Pros
    - Smaller, faster, lower power than FPGA or SoG/GA
    - Faster development time than full custom because a standard cell library is used as the basic building blocks of the design
  - Cons
    - Custom mask set is expensive
    - Resistance to add library elements
    - Economical only for
      - High volume or
      - High cost devices
  - Examples
    - AMIS SC13 standard cell

Standard Cell Layout



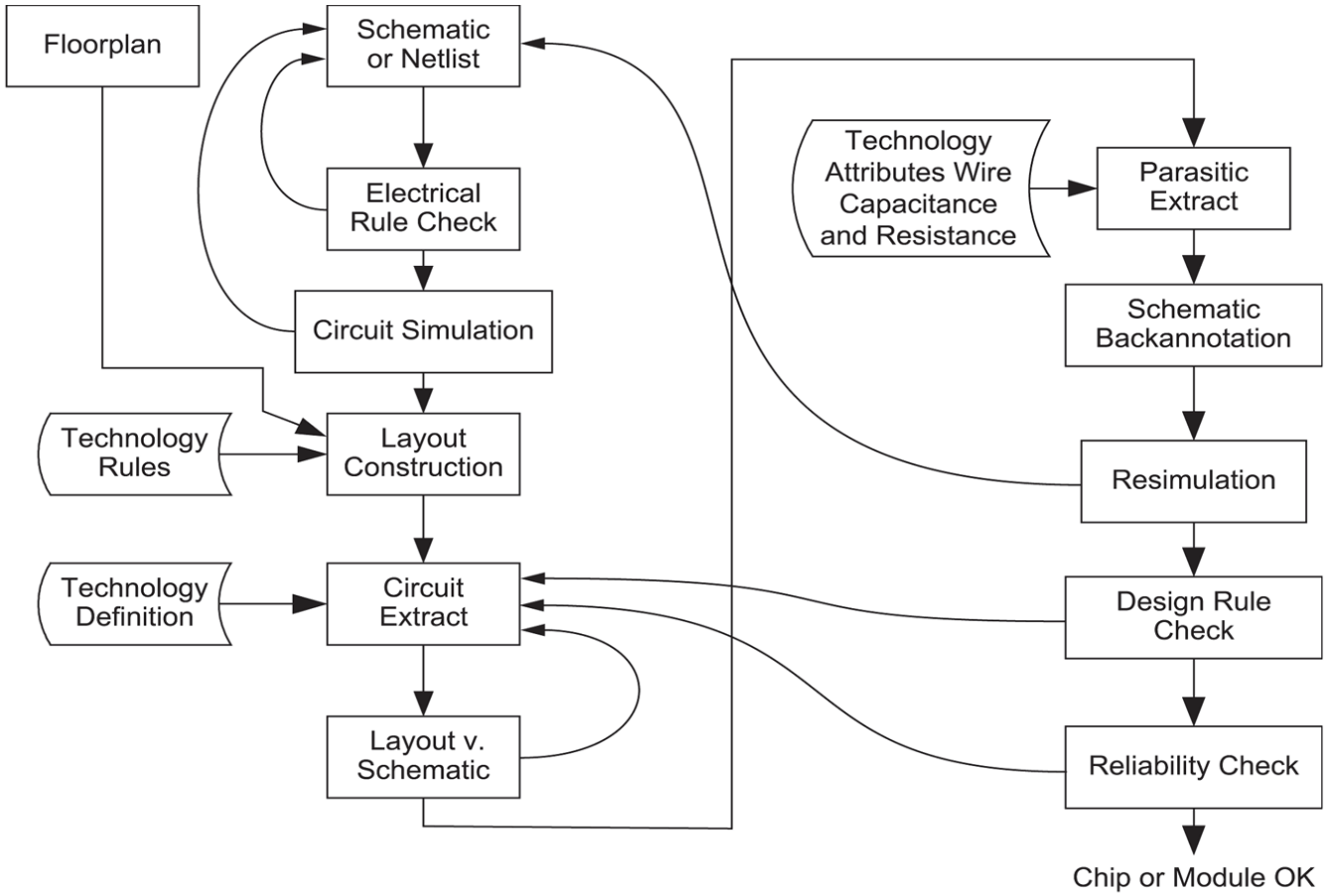
Standard Cell Library Example

Gate Type	Variations	Options
Inverter / buffer / tristate buffers		Wide range of power options, 1X, 2X, 4X, 8X, 16X, 32X, 64X minimum size inverter
NAND / AND	2–8 inputs	High, normal, low power
NOR / OR	2–8 inputs	High, normal, low power
XOR / XNOR		High, normal, low power
AOI / OAI		High, normal, low power
Multiplexers	Inverting/noninverting	High, normal, low power
Schmitt trigger		High, normal, low power
Adder / half adder		High, normal, low power
Latches		High, normal, low power
Flip-flops	D, with and without synch/asych set and reset, scan	High, normal, low power
I/O pads	Input, output, tristate, bidirectional, boundary scan, slew rate limited, crystal oscillator	Various drive levels (1–16 mA) and logic levels

Implementation Options

- Full Custom
  - Pros
    - Custom design at the physical level
    - Smallest, fastest, or lowest power circuit
      - You get exactly what you want
        - Or are capable of designing!
  - Cons
    - Design at physical level!
    - Custom mask set is expensive
    - Economical only for
      - High volume or
      - High cost devices
  - Examples
    - Microprocessor datapath, cache, IO cell

Custom Design Flow



CMOS Design Methods

Design Method	Non-recurring Engineering	Unit Cost	Power Dissipation	Complexity of Imple-mentation	Time to Market	Perfor-mance	Flexibility
Microprocessor/ DSP	low	medium	high	low	low	low	high
PLA	low	medium	medium	low	low	medium	low
FPGA	low	high	medium	medium	low	medium	high
Gate Array/SOG	medium	medium	low	medium	medium	medium	medium
Cell Based	high	low	low	high	high	high	low
Custom Design	high	low	low	high	high	very high	low
Platform Based	high	low	low	high	high	high	medium