55:131 Introduction to VLSI Design
Project #2 -- Fall 2010

Synthesize Simple PCI Target with EDAC
Due Date: Monday October 25, 2010

Introduction

In this project we will synthesize a simple Peripheral Component Interconnect (PCI) target device. Typical connection of the device in a system is shown in figure 1. A representative block diagram of the device is shown in figure 2. The source code for the design will be provided. The code uses a combination of structural and behavioral styles in VerilogHDL.

Code for the encode and decode blocks is provided by Xilinx application note XAPP 645, see http://www.xilinx.com/support/documentation/application_notes/xapp645.pdf

The synthesis tool provided in the Xilinx ISE webpack will be used in this project.

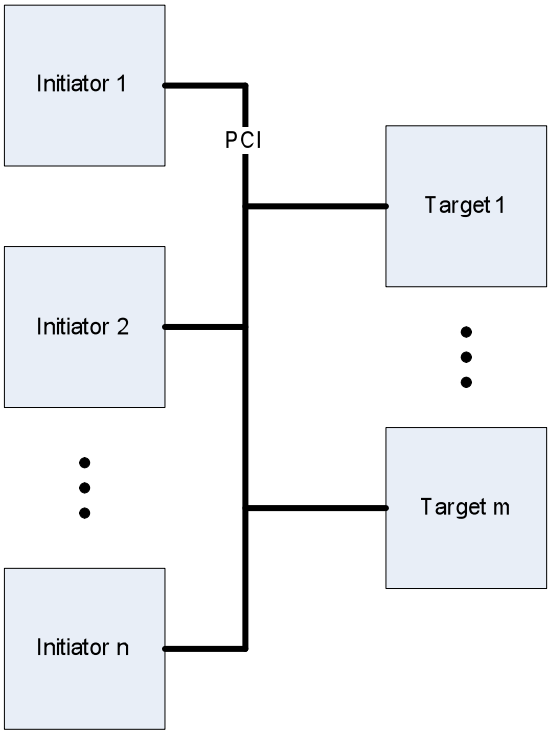

Figure 1 - PCI Bus System

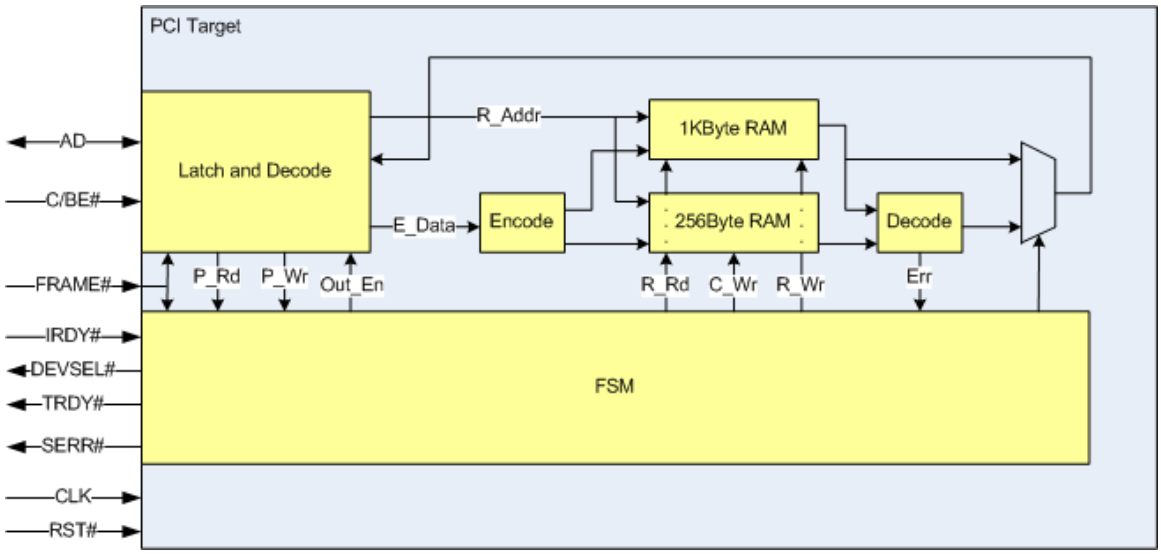

Figure 2 - Simple PCI Target with EDAC

Goals

- To synthesize the design and explain warnings from the synthesis tool.
- To understand synthesis constraints and enter them in the synthesis tool
- To evaluate speed/cost/area tradeoffs
- To find critical path within the design

Synthesis Parameters

- Target device: Xilinx Virtex-6 6VLX75TFF484, speed grade -1
- Clock speed constraints: 66.66MHz
- Input setup constraint: Input Delay = 12 nS
- Output clock-out constaint: Output Delay = 9 nS
- IO constraints: PCI drivers for all IO (done in layout tool)
- Pinout constraints: None

Discussion:

PCI timing system-level timing is shown in figure 3, below. The PCI target must support 66MHz timing.

$$T_{cyc} \geq T_{val} + T_{prop} + T_{skew} + T_{su}$$

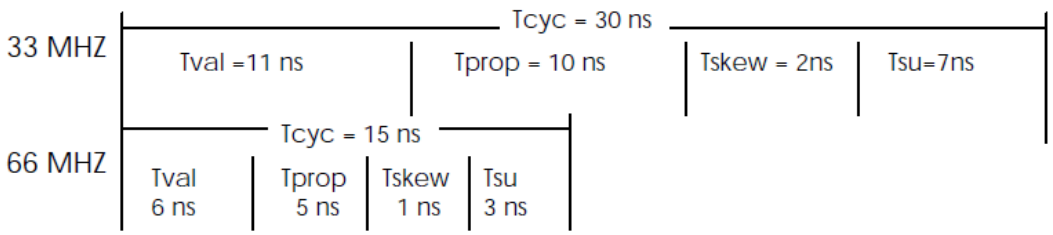

Figure 3 - PCI Timing

Use the Xilinx FPGA synthesis tool from Mentor Graphics to synthesize the PCI target. The design is completely synchronous. In other words, all flip-flops are clocked by the same CLK signal and reset or preset by the RST# signal. The memory for the PCI Target device is not initialized by the reset signal.

After adding the input files and setting up the design, compile it. At this point, any errors need to be reviewed and fixed. Warnings should be fixed as necessary. The Log File contains the error, warning, and information messages.

The design is synthesized using the Xilinx library information. The tool's output consists of different ways to view the design, a netlist, and several reports.

Questions

1. Explain all synthesis warnings.
2. What type of encoding is used for the fsm?
3. How are the memories implemented in the design (hints: read the Xilinx Virtex-6 documentation and area report for help)?
4. What is the maximum clock frequency of this design?
5. Does the design meet its internal timing requirements? Explain why or why not.
6. Does the design meet its IO timing requirements? Explain why or why not.
7. Locate the register-register (i.e. internal, not IO) critical path in the Verilog RTL.
8. Correlate the critical path delay to the maximum clock frequency reported by the tool.
9. What can be done to improve the critical path timing?
10. Are the input and output delay constraints correct? Why or why not?

What to turn in:

Turn in your netlist, area report, timing report(s), synthesis log file, and answers to the questions above. All files should be ascii text files that are zipped-up into one file. Place the file in the project 2 dropbox.

Discussion:

Use the Precision FPGA synthesis tool from Mentor Graphics to synthesize the PCI target. The design is completely synchronous. In other words, all flip-flops are clocked by the same CLK signal and reset or preset by the RST# signal. The memory for the Target device is not initialized by the reset signal.
